Digital Logic Design LAB #7 - VHDL

Objective
The objective of this lab is to introduce students to VHDL (Hardware Description Language) development environment in order to analyze and synthesize combinational and sequential logic.

Related Principles & Resources
- Combinational and sequential logic circuit design
- VHDL Reference Guide in the Active-HDL application (Help>Interactive VHDL Tutorial)

Equipment
- Windows-based PC
- Aldec Active-HDL Student Edition
- USB hard disk or other removable drives

Preparation
- All lab computers have Active HDL installed. Students can also download a free version of Aldec Active-HDL Student Edition from www.Aldec.com for personal use only. If you download from Aldec.com and follow the application instruction for installation, it is important to do the following before your first design:
  *** select "Tools→Preferences→Access to Design Objects". Uncheck "Limit read access to design top-level signals only" and check all three check boxes under "Enable Access". Then press "Apply" button. Now you are ready to enter and simulate your design. ***
- Review Lecture and text material on VHDL
- Use *"VHDL Entry Tutorial" in " help>online documentation" menu of Active HDL to familiarize yourself with Active HDL environment.*

Experiment #1
Design and create simulation waveform for an 8-bit even parity checker using VHDL. The system will accept 8-bit data and outputs a one if there are even numbers of ones, otherwise outputs zero. *(hint: xor is helpful)*

Experiment #2
Design and create simulation waveform for an 8-bit up/down synchronous binary counter using VHDL.

Experiment #3
Design and create simulation waveform for a 16-bit shift register using VHDL. This circuit will accept input at the rising edge of clock and outputs the input bit value after 16 full clock cycles.

Experiment #4
Design and create a simulation waveform for a 5 out of 16 event detector using VHDL. This system will assert output to 1 when exactly 5 out of the last 16 serial events (value of input at the rising edges of clock) have been 1s.

Report Requirements
All reports must be computer printed (Formulas and Diagrams may be hand drawn) and at minimum include:

For each Experiment
a) Clear problem statement; specify items given and to be found.
b) Identify the theory or process used.
c) Document resulting system diagram, code and simulation timing diagram and other relevant results.

For the report as a whole
a) Cover sheet with your name, course, lab, date of completion and team members' names.
b) Lessons Learned from the experiments.
c) A new experiment and expected results which provide additional opportunity to practice the concepts in this lab.