Digital Logic Design Lab #7 - Introduction to Verilog HDL

Using Aldec Active-HDL Development Environment

Objective

Introduce Verilog Hardware Description Language (Verilog) using Aldec Active-HDL Development Environment.

Preparation

It is important that you carefully read and complete the following steps before starting to work on the experiments in this lab:

1) Download and install Aldec Active-HDL Student Edition from:
   "https://www.aldec.com/en/products/fpga_simulation/active_hdl_student"
   Note: You only need to install the main set up file (do not download FPGA Libraries)

   Once Active-HDL has been installed, run the program and select from the menu Tools/Preferences/Simulation/Access to Design Objects. Uncheck "Limit read access to design top-level signals only" and click the three check boxes below it: "Read" "Read/Write" and "Enable Read/Write access for SLP accelerated nets" Click Apply and then click OK.

2) Complete reading and assignments in Chapter 7 - Verilog

3) Watch the following two videos:
   a) Introduction to Verilog at https://youtu.be/WML15LkhtYk
   b) Active-HDL Verilog Tutorial at https://youtu.be/aHjJ4XWvTnw
   Notes:
   1) If you have problems with simulation waveform see https://youtu.be/xo9zuasE_9w
   2) *Active-HDL user interface (Icons and menu items) maybe different in each version*

Now, you are ready to start on Experiments…

Experiment #1 – Parity Checker

Design and create simulation waveform for an 8-bit even parity checker using Verilog. The system will accept 8-bit data and outputs a one if there are even numbers of ones, otherwise outputs zero. *(hint: use xor function)*

Experiment #2 – Binary Counter

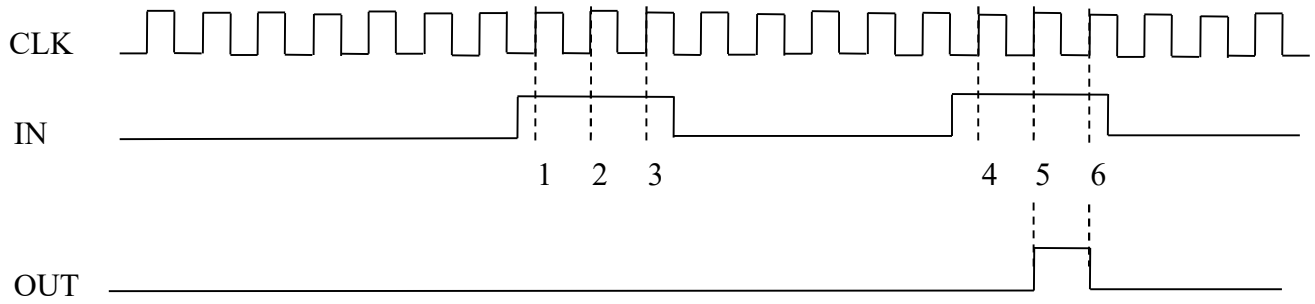
Design and create simulation waveform for an 8-bit up/down synchronous binary counter using Verilog.

Experiment #3 – Shift Register

Design and create simulation waveform for a 16-bit shift register using Verilog. This circuit will accept input at the rising edge of clock and outputs the input bit value after 16 full clock cycles.

Experiment #4 – Event Detector

Design and create a simulation waveform for a 5 out of 16 event detector using Verilog. This system will assert output to 1 when exactly 5 out of the last 16 serial events (value of input at the rising edges of clock) have been 1s. Here is an example timing diagram:



Hint: You may the find the video at the following link helpful: https://youtu.be/A5ebM9Cfgfk

Report Requirements

All reports must be computer printed (Formulas and Diagrams may be hand drawn) and at minimum include:

For each Experiment

a) Clear problem statement: specify items given and to be found.
b) Identify the theory or process used.
c) Document resulting system diagram, code and simulation timing diagram and other relevant results.

For the report as a whole

a) Cover sheet with your name, course, lab, date of completion and team members' names.
b) Lessons Learned from the experiments.
c) A new experiment and expected results which provide additional opportunity to practice the concepts in this lab.