Digital Logic Design Lab #7 Introduction to Verilog – Xilinx ISE

Objective
The objective of this lab is to introduce students to Verilog Hardware Description Language (Verilog) development environment in order to analyze and synthesize combinational and sequential logic.

Related Principles & Resources
- Combinational and sequential logic circuit design
- Review Lecture and text material on Verilog
- Data entry and simulation
- Selected Computers in the lab have Xilinx ISE WebPACK Installed. Students can also download a free version of Xilinx ISE WebPack and install it on their personal computer. License is free for personal use only.
- USB hard disk or other removable drives

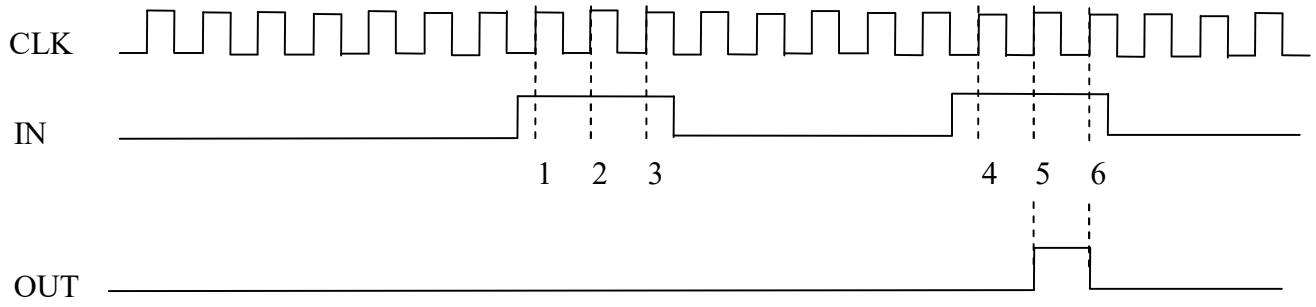
Experiment #1
Complete Section 1 and 2 of "Introduction to Verilog and FPGA Design using Xilinx ISE WebPACK" located at https://www.engrcs.com/courses/engr250/labs/XilinxISEwebpack&MimasFPGAintro.pdf.

Experiment #2
Design and create simulation waveform for an 8-bit even parity checker. The system will accept 8-bit data and outputs a one if there are even numbers of ones, otherwise outputs zero. *(hint: xor is helpful)*

Experiment #3
Design and create simulation waveform for an 8-bit up/down synchronous (rising edge of clock) binary counter using Verilog.

Experiment #4
Design and create simulation waveform for a 8-bit shift register using Verilog. This circuit will accept input at the rising edge of clock and outputs the input bit value after 8 full clock cycles.

Experiment #5
Design and create a simulation waveform for a 5 out of 16 event detector using Verilog. This system will assert output to 1 when exactly 5 out of the last 16 serial events (value of input at the rising edges of clock) have been 1s. Here is an example timing diagram:



Report Requirements

All reports must be computer printed (Formulas and Diagrams may be hand drawn) and at minimum include:

For each Experiment

a) Clear problem statement; specify items given and to be found.
b) Identify the theory or process used.
c) Document resulting system diagram, Verilog code, test code, simulation timing diagram and other relevant material.

For the report as a whole

a) Cover sheet with your name, course, lab, date of completion and team members' names.
b) Lessons Learned from the experiments.
c) A new experiment and expected results which provide additional opportunity to practice the concepts in this lab.