Digital Logic Design LAB #8

Objective
Experience with analyzing and synthesizing sequential logic circuit using VHDL.

Related Principles & Resources
- Combinational and sequential logic circuit design
- VHDL Reference Guide in the Active-HDL application (Help>Interactive VHDL Tutorial)

Equipment
- Windows-based PC
- Aldec Active-HDL Student Edition
- USB hard disk or other removable drives

Supplies
- None

Preparation
- Review Lecture and text material on VHDL
- Complete Hierarchy/Block Diagram

Experiment #1
Design and create simulation waveform for a 9-count up-down ring counter in VHDL.

Experiment #2
A three way intersection is in need of a traffic signal control system and you have been assigned the task to design and implement the system. Each direction has only one lane and one signal control light (Green and Red) per lane. The right hand rule of driving applies to the intersection. Further you have to give only one lane go or green light at a time.

Design and create simulation waveform for the three way intersection control system using VHDL.

Report Requirements
All reports must be computer printed (Formulas and Diagrams may be hand drawn) and at minimum include:

For each Experiment
a) Clear problem statement; specify items given and to be found
b) Identify the theory or process used
c) Documents resulting block diagram, code, simulation screen shots, timing diagrams and other results.

For the report as a whole
a) Cover sheet with your name, lab, date of completion and team members' names
b) Lessons learned from this lab
c) Content/Format improvement suggestions and reason for the suggestions