Digital Logic Design Lab #8 FPGA Implementation/Synthesize

Objective

The objective of this lab is to implement/synthesize circuits using Verilog Hardware Description Language (Verilog) to describe the circuit behavior and FPGA to implement the circuit/hardware.

Related Principles & Resources

- Combinational and sequential logic circuit design
- Review Lecture and text material on Verilog
- Selected Computers in the lab have Xilinx ISE WebPACK Installed. Students can also download a free version of Xilinx ISE WebPack and install it on their personal computer. License is free for personal use only.
- USB hard disk or other removable drives
- Review of "Introduction to Verilog and FPGA Design using Xilinx ISE WebPACK" located at https://www.engrcs.com/courses/engr250/labs/XilinxISEwebpack&MimasFPGAintro.pdf.
- Mimas Spartan 6 FPGA Development Board (obtain from your instructor) https://www.engrcs.com/courses/engr250/labs/MimasSpartan6FPGABoard.pdf .
  Note: Never use power supply when working with Mimas Board.

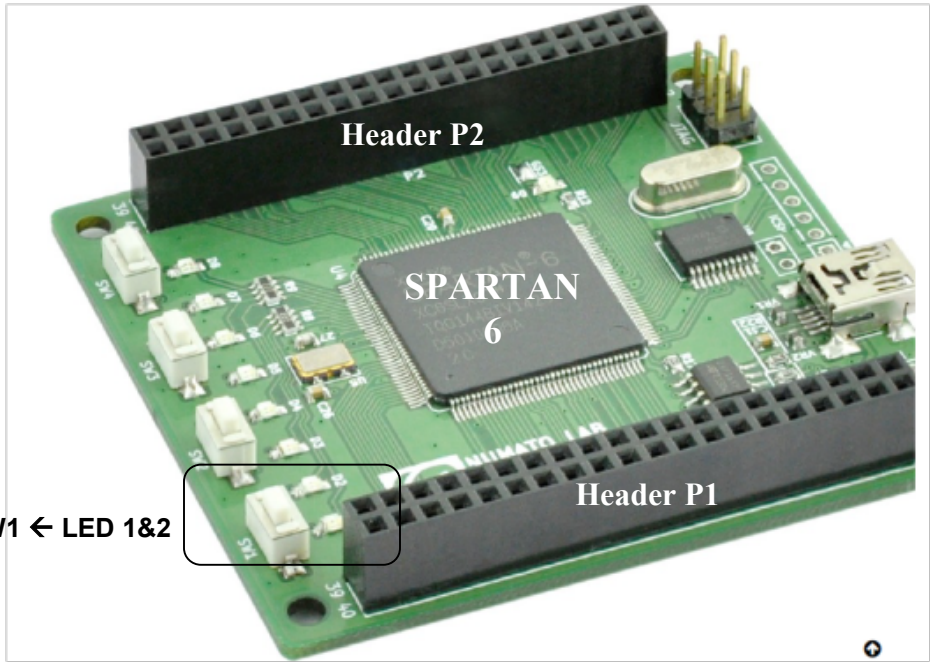
Experiment #1

Complete all sections of "Introduction to Verilog and FPGA Design using Xilinx ISE WebPACK" located at https://www.engrcs.com/courses/engr250/labs/XilinxISEwebpack&MimasFPGAintro.pdf. Demonstrate the functionality on Mimas Spartan 6 FPGA Development Board.

NOTE: Never use power supply when working with Mimas Board.

Experiment 2

Design and implement on Mimas FPGA Development Board the ability to turn on LEDs 1 and 2 for 1 second in response to pressing SW1.



The Board has a 100 MHz built-in clock that is connect to SPARTAN at pin 126. So by adding the following statement to your design's .ucf file, you get access to CLK period of 10^{-8} seconds (50% duty cycle).

NET "CLK" LOC = P126;

Adding the following to your .ucf file give you access to LED1-8 and SW1-4

```
NET "LED1"    LOC = P119    | IOSTANDARD = LVCMOS33 | DRIVE = 24 | SLEW = FAST;
NET "LED2"    LOC = P118    | IOSTANDARD = LVCMOS33 | DRIVE = 24 | SLEW = FAST;
NET "LED3"    LOC = P117    | IOSTANDARD = LVCMOS33 | DRIVE = 24 | SLEW = FAST;
NET "LED4"    LOC = P116    | IOSTANDARD = LVCMOS33 | DRIVE = 24 | SLEW = FAST;
NET "LED5"    LOC = P115    | IOSTANDARD = LVCMOS33 | DRIVE = 24 | SLEW = FAST;
NET "LED6"    LOC = P114    | IOSTANDARD = LVCMOS33 | DRIVE = 24 | SLEW = FAST;
NET "LED7"    LOC = P112    | IOSTANDARD = LVCMOS33 | DRIVE = 24 | SLEW = FAST;
NET "LED8"    LOC = P111    | IOSTANDARD = LVCMOS33 | DRIVE = 24 | SLEW = FAST;
NET "SW1"     LOC = P124    | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;
NET "SW2"     LOC = P123    | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;
NET "SW3"     LOC = P121    | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;
NET "SW4"     LOC = P120    | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;
```

Note: Complete definition of all header pins on the Board to SPARTAN-6 pins is available in mimas.ucf file at https://numato.com/product/mimas-spartan-6-fpga-development-board.

Start by writing a Verilog module with input SW1 and CLK, and output of LED1 and LED2.

You can create an always block that waits for SW1 transition from pressed (Logic 0) to released (logic 1). You can set LED1 and LED2 to logic "1" when SW1 release is detected,.

To wait for 1 second use input clk (period =10^{-8} second). Use an always block that triggers on falling edge of clock and count 100,000,000 clk cycles. At this point you may turn off the LEDs by setting them to '0'.

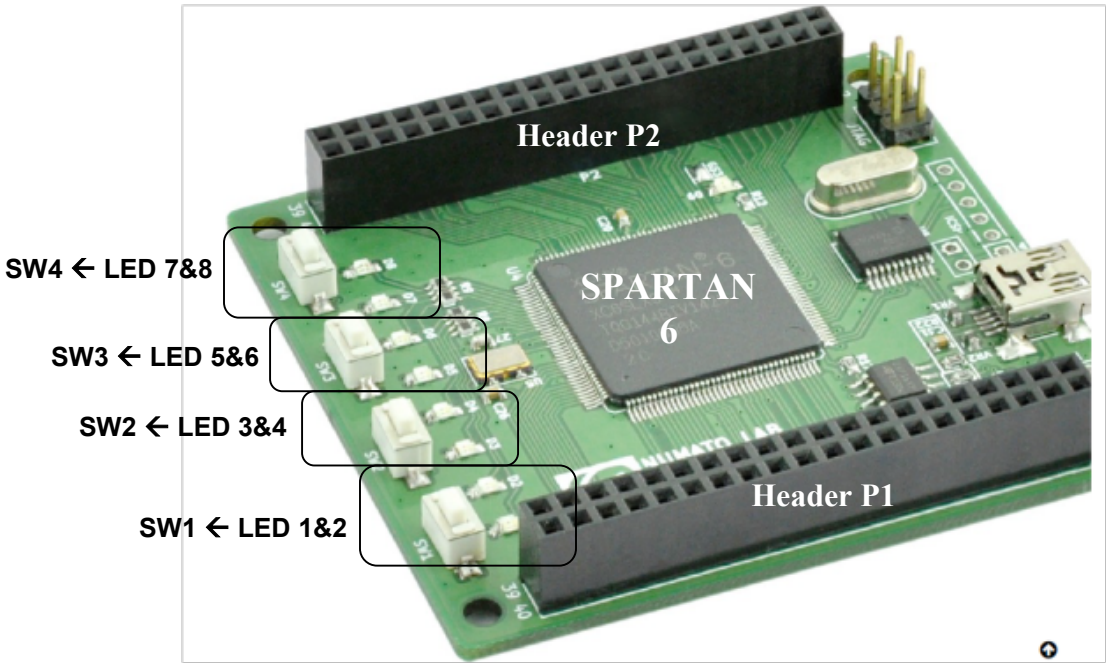
In your test bench code, you can use the following to simulate the clock but you may want to reduce your count to 10.

```
reg clk
always begin  #5 clk=~clk;  end
```

Use the information provide in this experiment along with the process used in experiment 1 to implement and test your design implementation on SPARTAN-6.

Experiment 3

Design and implement a game to test player's reflexes on Xilinx SPARTAN-6 using the available 4 momentary switches (SW1-4) and corresponding 8 LEDS (D1-8) on Mimas FPGA Development Board.



Player may start the game by pressing SW1 momentarily – the game will start 1 second after the SW1 is released. During the game player is expected to press the switch corresponding to the LED that is on. Each successive level expect player to react faster as shown below.

Level 1 – Player must momentarily press the correct button within 2 second of associate LED turn on.
Level 2 – Player must momentarily press the correct button within 1 second of associate LED turn on.
Level 3 - Player must momentarily press the correct button within 1/2 second of associate LED turn on.
Level 4 - Player must momentarily press the correct button within 1/4 second of associate LED turn on.
Level 5 - Player must momentarily press the correct button within 1/8 second of associate LED turn on.
Level 6 - Player must momentarily press the correct button within 1/16 second of associate LED turn on.

The game stops if user presses the wrong key or takes longer than allowed. After the game stops, number of LEDs that are on indicates the highest level achieved by the player.

Pressing SW1 momentarily starts a new game.

Demo your solution for the instructor and obtain an approval signature to be included in your report.

Include the approval signature in your report:

Team Members: • • • •	LAB8 Demo Instructor Approval Signature & Date:

What's Next

Congratulation, you have completed a FPGA design process from idea to actual working circuit and hardware. Next, you can add an LCD display, speakers via Header pin to display game statistics and messages.

Report Requirements

All reports must be computer printed (Formulas and Diagrams may be hand drawn) and at minimum include:

For each Experiment

d) Clear problem statement; specify items given and to be found.
e) Identify the theory or process used.
f) Document resulting system diagram, Verilog code, test code, simulation timing diagram and other relevant material.

For the report as a whole

d) Cover sheet with your name, course, lab, date of completion and team members' names.
e) Lessons Learned from the experiments.
f) A new experiment and expected results which provide additional opportunity to practice the concepts in this lab.