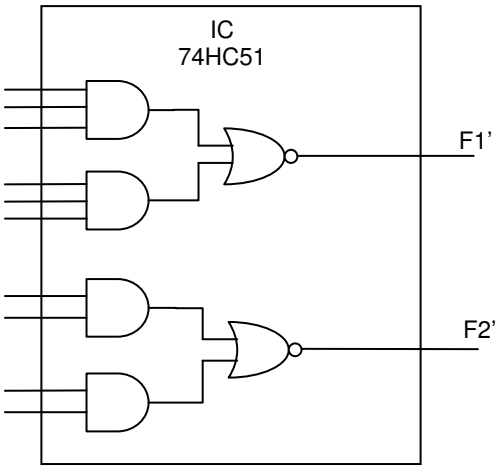
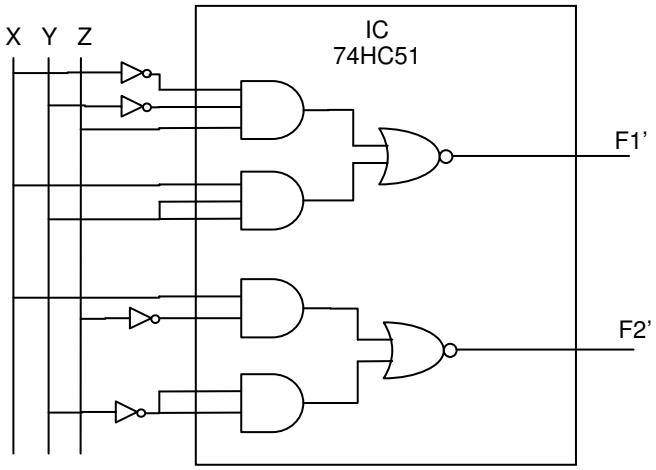
Digital Logic Design - Chapter 9

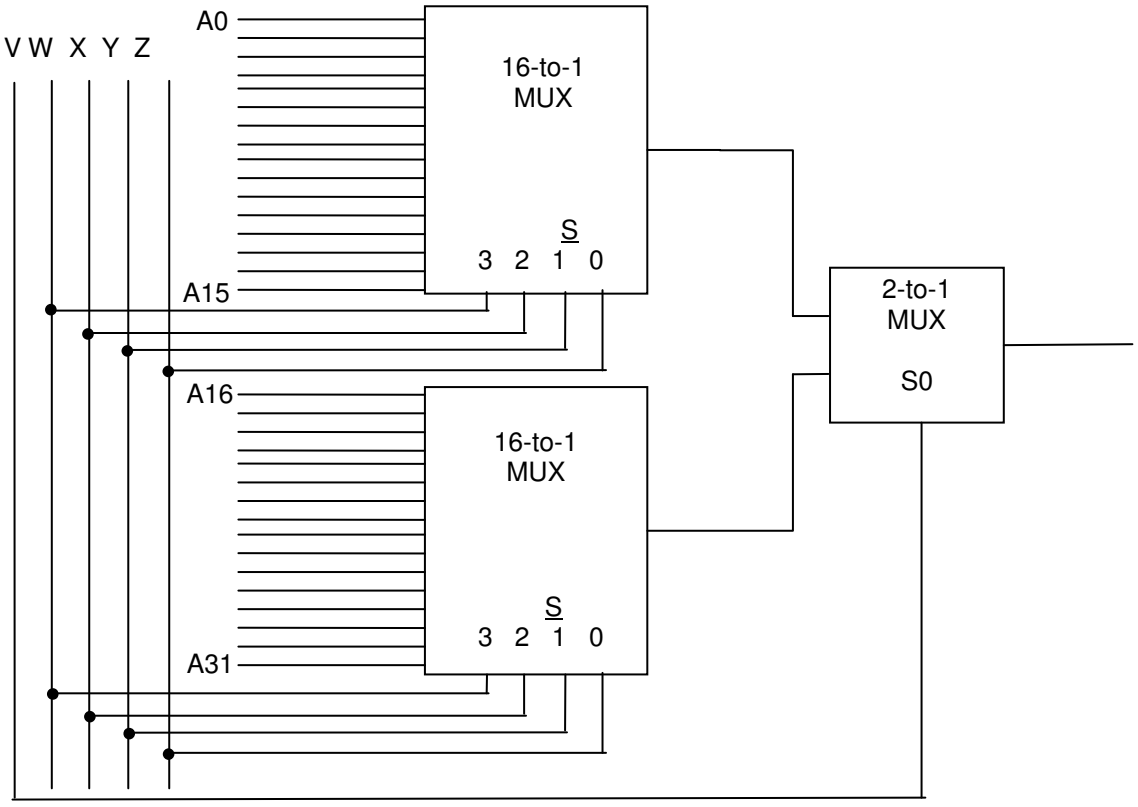
1. Design a circuit to realize the logic functions F1 = X'.Y'.Z + X.Y and F2 = Y' + X.Z' using the IC shown below. Assume all signals are uncomplemented positive-logic signals and use inverters as necessary.



Solution



2. Use two 16-bit multiplexers and one 2-bit multiplexer to construct a 32-bit MUX.



Solution

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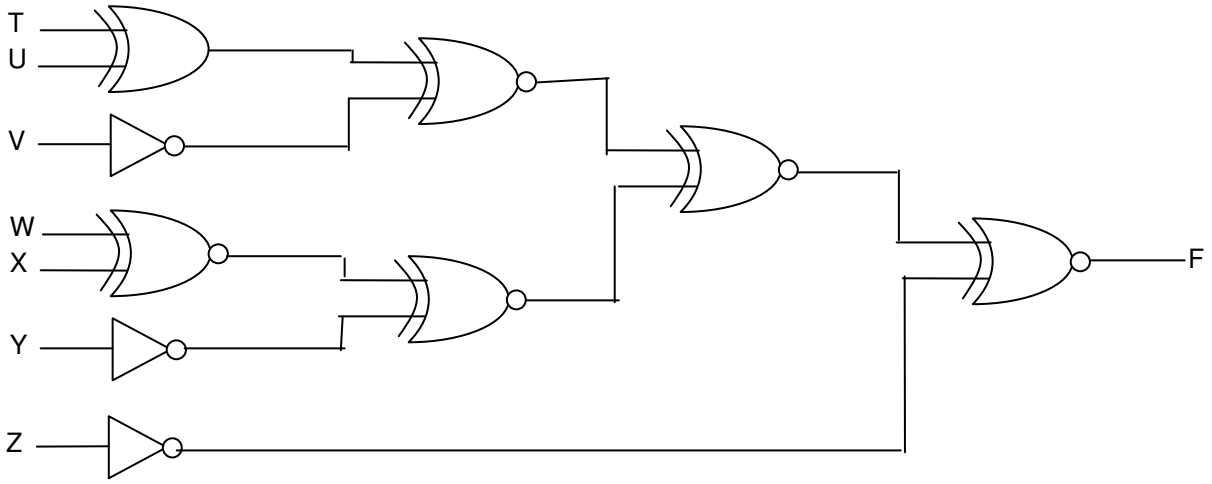
3. For the following circuit, determine if the output function is odd or even.



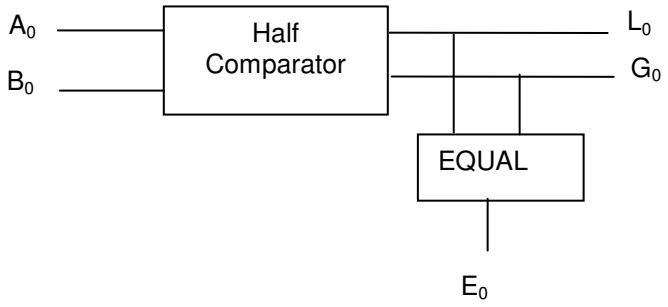
Definitions:

- An odd function will output a 1 when there is an odd number of 1s (1, 3, 5 …) in the input (XOR of all inputs).
- An even function will output a 1 when there is an even number of 1s (2, 4, 6 …) in the input (XNOR of all inputs).

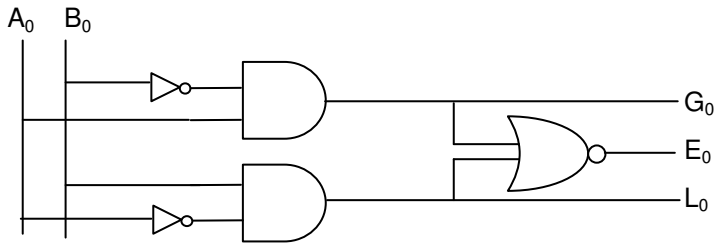
Solution

Function F is the XOR of all input functions and therefore is an odd function.

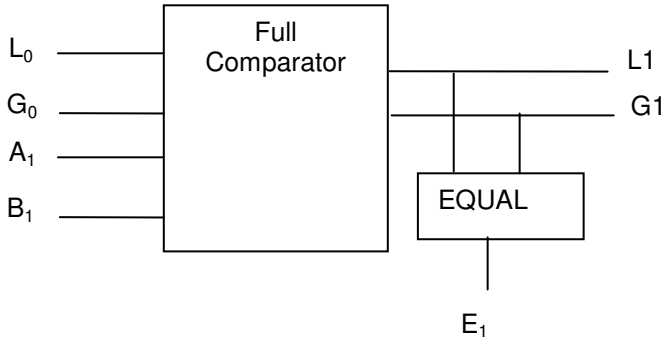
4. Design the half-comparator represented by the block diagram shown below. L_0 represents $A_0<B_0$, G_0 represents $A_0>B_0$, and E_0 represents $A_0=B_0$. Determine E_0 from $L_0 = G_0=0$.



Solution



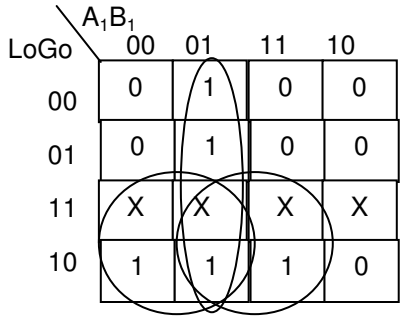
5. Design a full comparator represented by the block diagram shown in figure below. L_0 represents $A_0<B_0$, G_0 represents $A_0>B_0$, L_1 represents $A_1A_0< B_1B_0$, G_1 represents $A_1A_0> B_1B_0$, and E_1 represents $A_1A_0= B_1B_0$. Determine E_1 from $L_1 = G_1=0$.



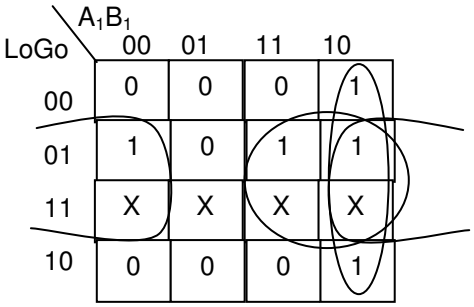
Solution

Input				Output	
Lo	**Go**	**A1**	**B1**	**L1**	**G1**
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	1	0

0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	Not Valid – X			



L1 = Lo.A1' + Lo.B1 + A1'.B1



G1 = Go.A1 + G0.B0'+A1.B1'

E1 = (L1 + G1)'

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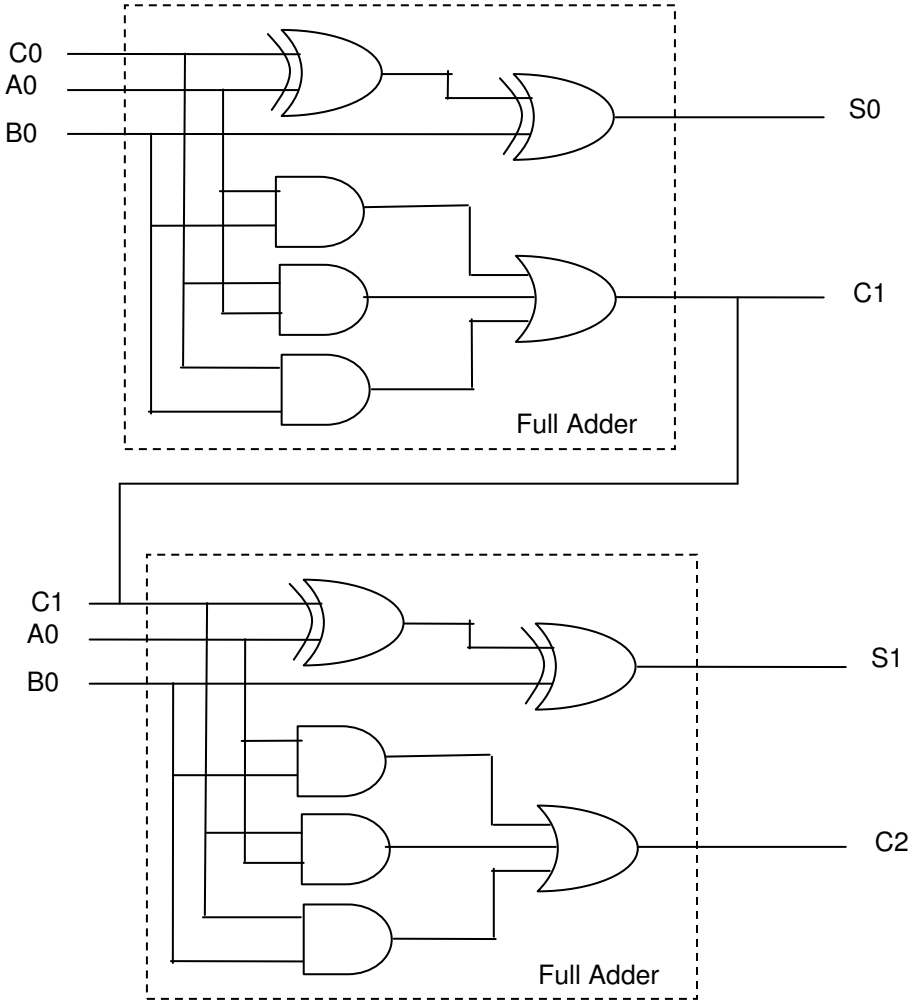
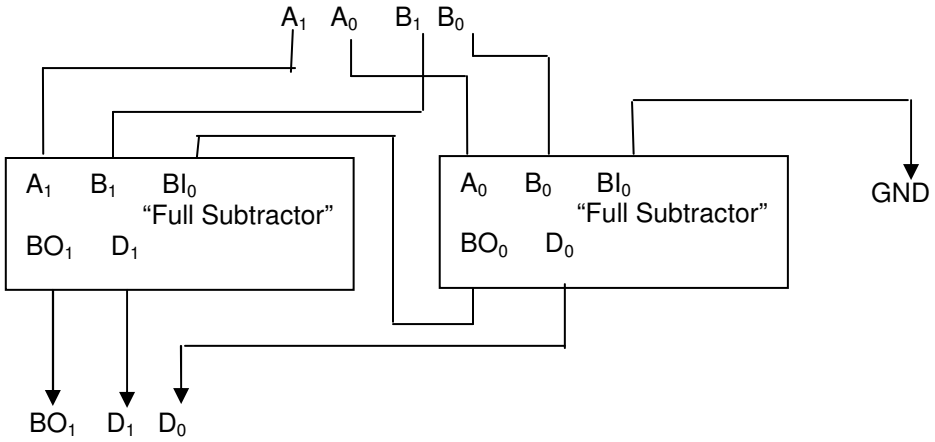
6. Design a gate-level 2-bit full adder that adds A1 A0, B1 B0 (2-bit numbers), and C0 (carry out) to obtain C2 S1 S0.

Solution



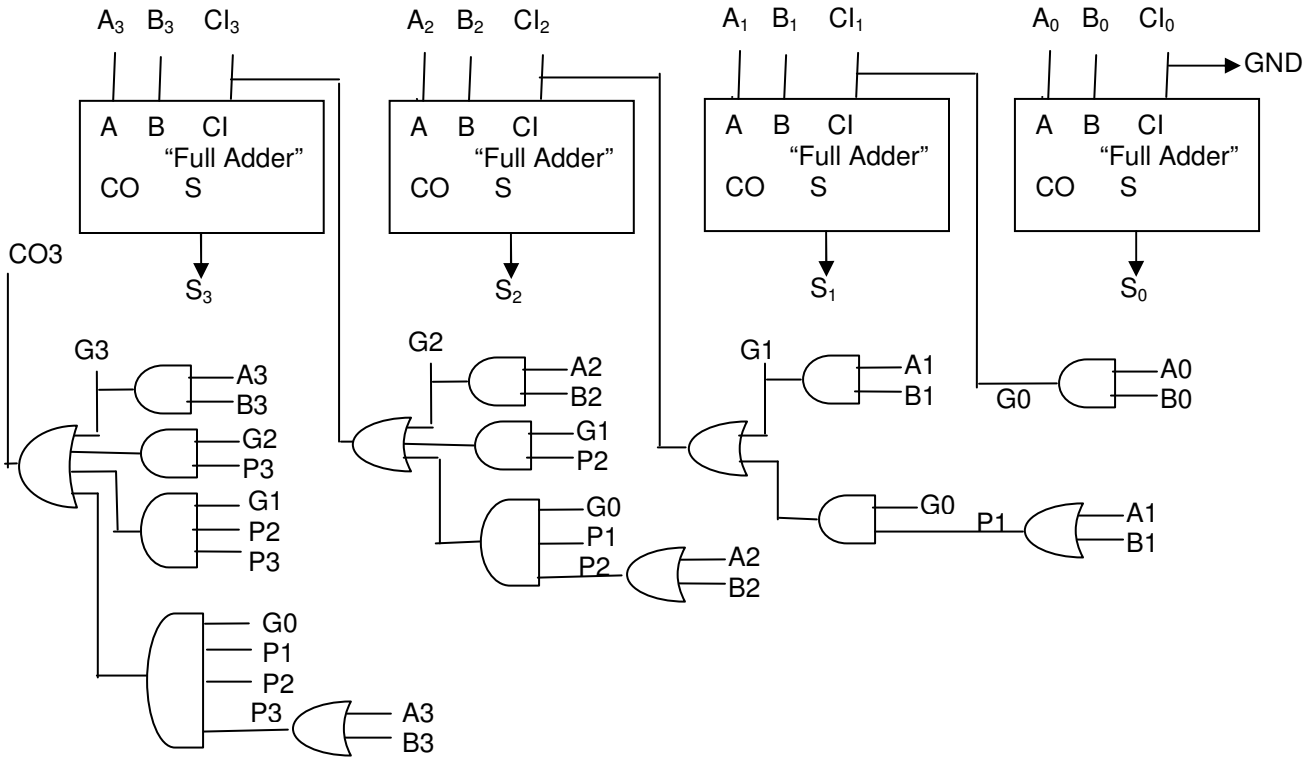
7. Design a modular 2-bit full subtractor using two 1-bit full subtractors.

Solution



8. Design a modular 4-bit full adder using four 1-bit full adders with carry look-ahead circuitry.

Solution



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9. Obtain a modular circuit design for a 4-bit x 4-bit binary multiplier using two-operand adders. Before you begin the design, calculate:

a) the number of result bits required.
b) the number of AND gates required.
c) the number of rows of independent adders required.
d) the number of bits in each independent adder.

Solution

Let the m bits be A3…A0 and the n bits be B3 …B0, where m is the number of multiplicand bits and n is the number of multiplier bits. Show your design with all connections made from the gates to the inputs of the adders.

a) The number of result bits = m+n=4+4=8
b) The number of AND gates = m x n = 4 x 4 = 16
c) The number of rows of independent adders = n – 1 = 4 – 1 = 3
d) The number of bits in each independent adder = m = 4

```
          A3  A2  A1  A0        Multiplicand (m-bits)
        X B3  B2  B1  B0        Multiplier (n-bits)
      ---------------------
          P30 P20 P10 P00       Partial Product 0
    + P31 P21 P11 P01           Partial Product 1
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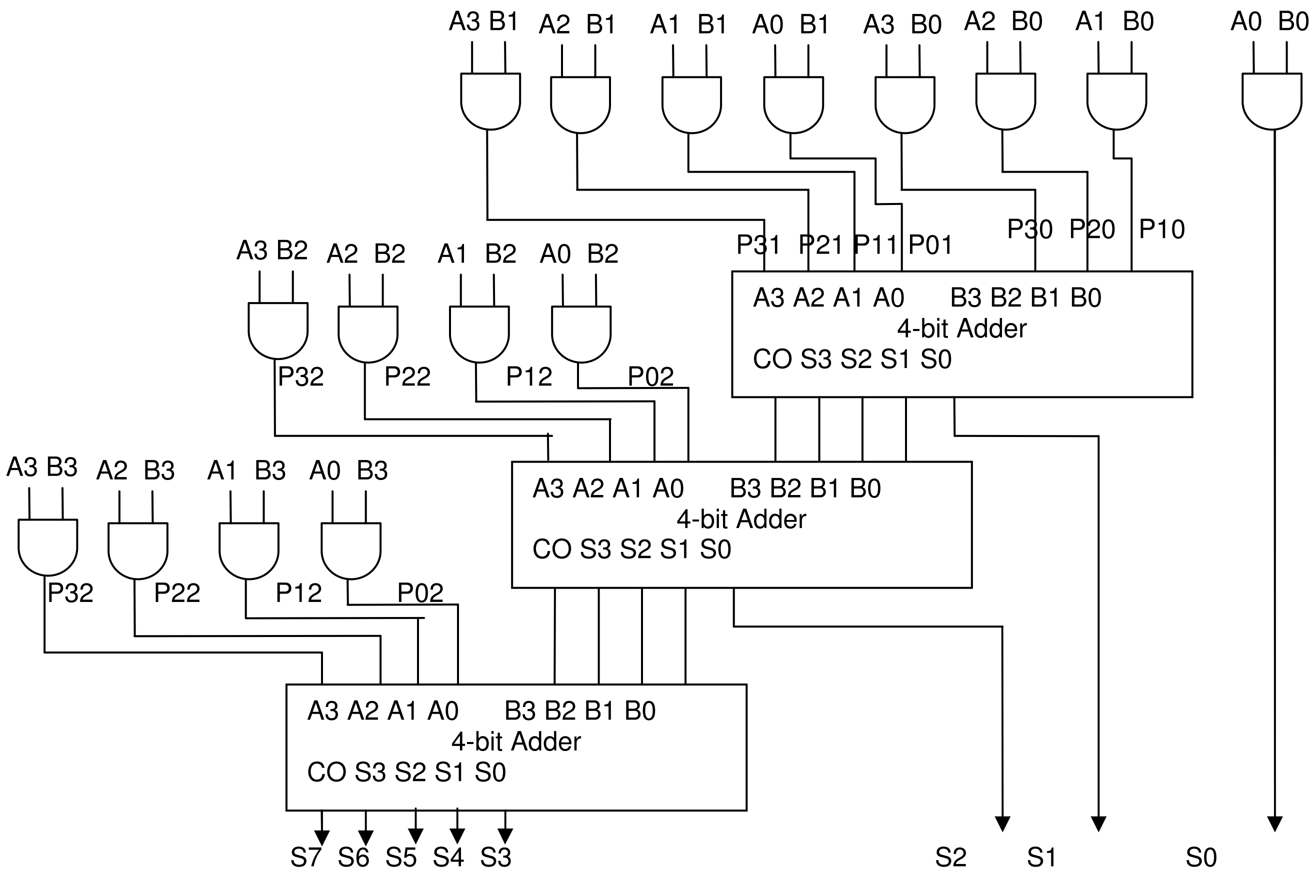
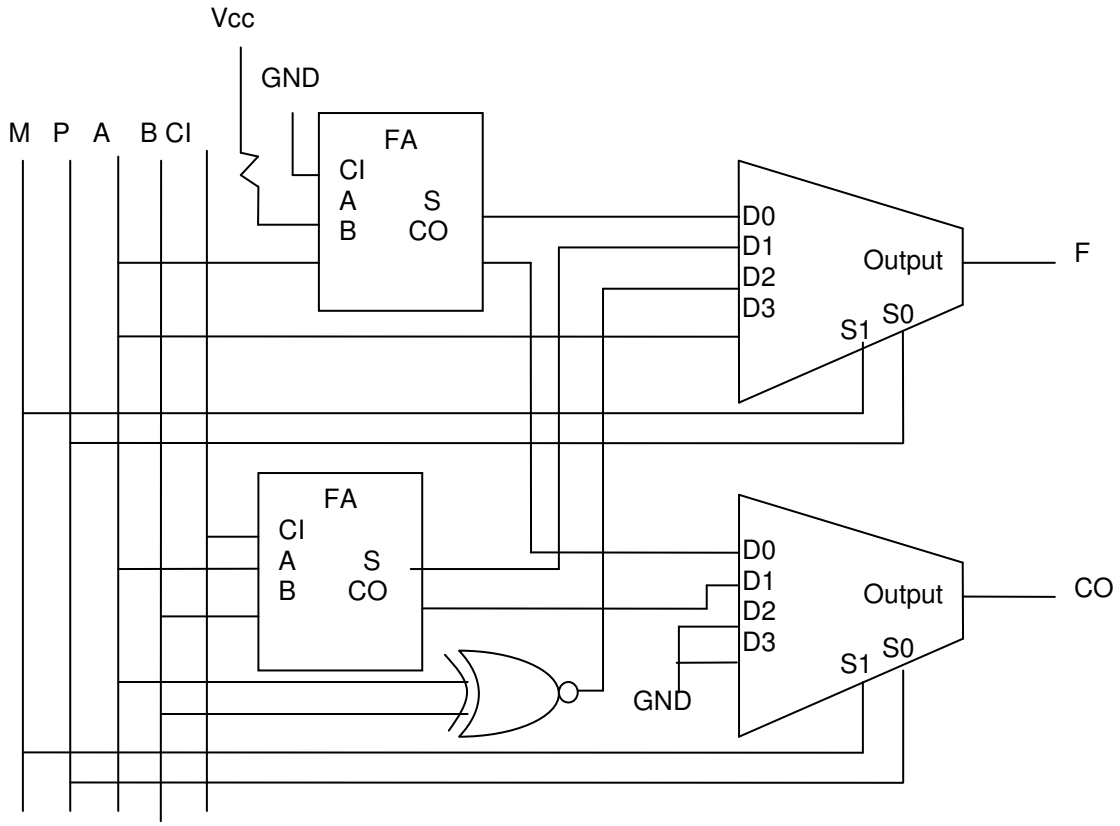
		S50	S40	S30	S20	S10	S00	Partial Sum 0
+	P32	P22	P12	P02				Parial Product 2
S61	S51	S41	S31	S21	S11	S01		Partial Sum 1
+ P33	P23	P13	P03					Parial Product 3
R7 R6	R5	R4	R3	R2	R1	R0		Partial Sum 2 (Result)



10. Design a single-bit ALU, using the modular design process, that will perform the following specification:

Selection		Arithmetic/Logic Operation
M	P	CO F
0	0	Increment A
0	1	A plus B plus CI
1	0	A = B
1	1	Transfer A

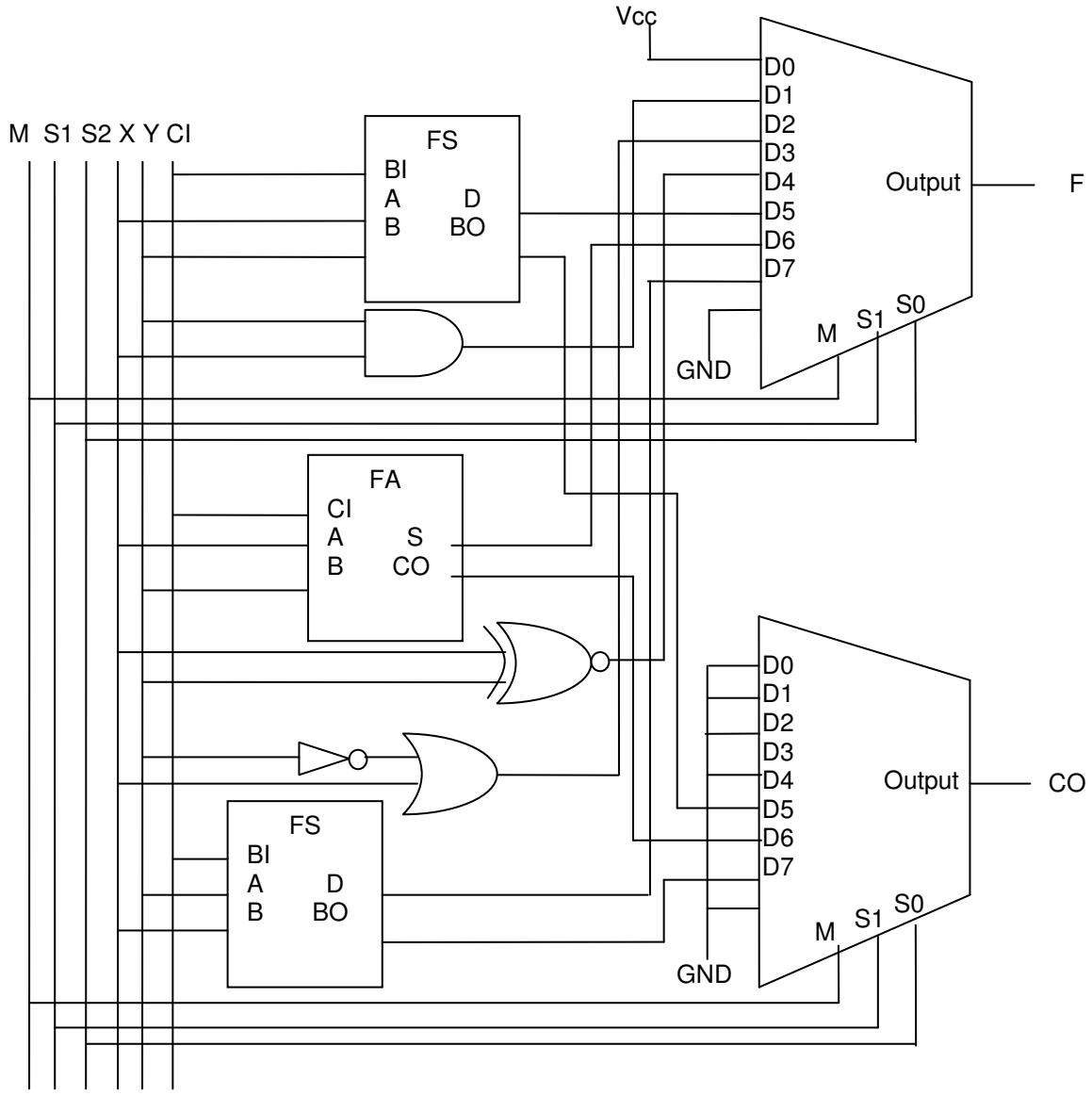
Solution



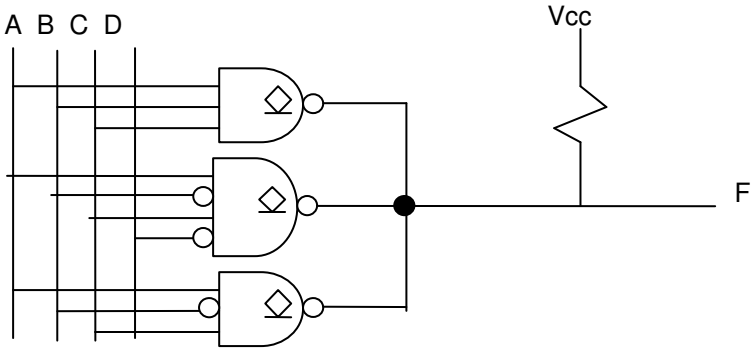
11. Design a single-bit ALU, using the data-flow modular design process, that will perform the following specification:

Selection			Arithmetic/Logic
M	S1	S0	Operation
0	0	0	PRESET
0	0	1	X.Y
0	1	0	X + Y'
0	1	1	X_{XNOR} Y
1	0	0	X MINUS Y
1	0	1	X PLUS Y
1	1	0	Y MINUS X
1	1	1	CLEAR

Solution



12. Is the circuit shown below a valid design? Explain your answer. If the answer is yes, write the Boolean expression for F(A, B, C, D).



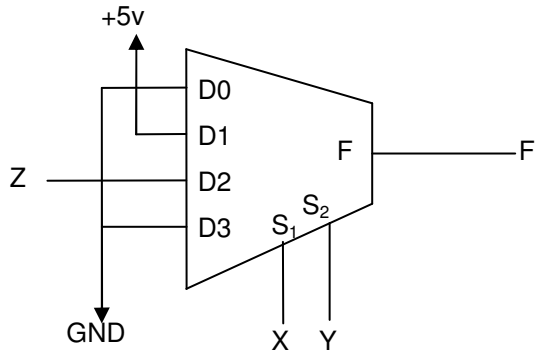
Solutions

Yes, Open Collector with Wired AND
F(A, B, C, D) = (A.B.C)'.(A.B'.C.D')'.(A.B'.C)'
Or apply DeMorgan Theorem → F' = A.B.C + A.B'.C.D' + A.B'.C

Problem 13
Design a logic circuit to implement the following function using only one 4-to-1 MUX and power supply with as many wires as needed.

$$F(X,Y,Z) = \pi\ (0, 1, 4, 6, 7)$$

Solution:



X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Problem 14
Design an 8-bit binary subtractor (S = A – B) using 1-bit full adder modules and other logic gates as required.
Note: 1-Bit Adder input include two 1-bit operands and carry in, its output is the sum and carry out.

Solution: